REMARKS

This Response is being submitted in response to the Office Action mailed November 13, 2006.

Claims 1, 3-7, and 9-27 are pending in the application. According to the Office Action, the rejections from the Office Action of January 17, 2006 are maintained and incorporated in this Office Action. Thus, claim 1 stands provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of co-pending Application No. 10/803,690. Claims 1-21 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over U.S. 5,682,519 to Saldanha, *et al.* (hereinafter "Saldanha") in view of U.S. 4,792,909 to Serlet (hereinafter "Serlet"). Claims 22-27 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Saldanha in view of Serlet and further in view of U.S. 6,385,757 to Gupta (hereinafter "Gupta"). Applicant respectfully traverses the Examiner's rejections.

Reconsideration of the claims is respectfully requested in view of the remarks below.

I. Double Patenting

Claim 1 stands provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of co-pending Application No. 10/803,690. Applicant hereby submits a terminal disclaimer for co-pending Application No. 10/803,690.

II. Claims 1-21

Claims 1-21 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Saldanha in view of Serlet. To establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest all of the claim limitations. Respectfully, neither Saldanha nor Serlet alone or when combined teaches or suggests all the claim limitations of claims 1 and 3-21. Claim 2 was previously cancelled, and the rejection of claim 2 is thus moot.

In claim 1, as amended, Applicant claims "[a] processor comprising: a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit

is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations; [and] a plurality of registers, wherein the plurality of registers include an instruction register, a next operation address register, and an end of OR address register." Neither Saldanha nor Serlet teach or suggest "[a] processor comprising: a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations; [and] a plurality of registers, wherein the plurality of registers include an instruction register, a next operation address register, and an end of OR address register."

Saldanha teaches building a circuit to physically represent a particular Boolean expression. Certain portions of the circuit are omitted to save power if they do not affect the result, i.e., the data path changes. Saldanha modifies the data path to use only the minimum number of components required to compute a predetermined operation or computation. *See, e.g.*, Saldanha, Col. 6:6-42. The circuit is not "formed in a static circuit with a static data path" and is unable to "dynamically perform the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations" as Applicant has claimed in claim 1.

In Saldanha's circuit, the electrical signal must propagate through the entire circuit that represents the entire Boolean expression. The short-circuiting described in Saldanha is a means for optimizing a data path for an expression. The circuit still must evaluate all data input to the circuit. *See, e.g.*, Saldhana, Col. 8:47-64. In contrast, Applicant claims a process for short-circuiting based on the data that is provided to the Boolean logic unit, i.e., the process eliminates evaluations when the inputs dictate that the overall result of the expression or conjunct can be short-circuited.

The Office Action states, "Saldanha also taught that his system was run on Sun Unix operating system, and the low power synthesis module was part of Sequential Interactive system software." *Office Action*, page 4. And "it can be seen easily that Saldanha's shod (sic) circuit evaluation was based on interactive software, and an interactive software, as already known in the art, was able to respond whenever the user's request occurred, and therefore, it was dynamic." *Id.* However, the section of Saldahna cited by the Office Action refers to the software used to design the physical circuit. Once

the software is used to design the circuit, and the circuit is built, the resulting circuit is static and unable to "dynamically perform the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations" as Applicant has claimed in claim 1. It is unclear how the fact that the circuit design software may be interactive is relevant to the circuits ability to "dynamically perform the short-circuit evaluation."

Serlet is introduced as teaching a "static Boolean circuit." *See* Office Action, page 4. Serlet does not cure the deficiencies of Saldanha. As discussed above, and pointed out by the Examiner, Saldanha teaches software for synthesizing a circuit based on a Boolean expression. Further, the Examiner states that Serlet teaches a static Boolean circuit. However, neither reference individually, nor the references in combination, teaches a circuit capable of dynamically short-circuiting itself based on an input sequence.

The claimed invention is capable of dynamically reconfiguring itself, by short-circuiting unnecessary circuit elements, based on an input. In contrast, Saldanha would require the re-synthesis of a new circuit for each boolean expression. Even if the circuits generated by Saldanha incorporated a static circuit, a new circuit would need to be optimized and generated for each boolean sequence. This is different than dynamically eliminating, by short-circuiting, unnecessary elements of a static circuit based on an input sequence. In other words, a circuit according to the present invention is capable of re-configuring itself on the fly based on the input data. Saldanha, even in combination with Serlet, would require the synthesis of a wholly-new circuit. Thus, claim 1 is patentable over Saldanha in view of Serlet. Claims 3-7, 9-12, and 13-21 depend from claim 1 and are patentable for at least the same reasons. Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 3-7, 9-12, and 13-21.

III. Claims 22-27

Claims 22-27 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Saldanha in view of Serlet and further in view of Gupta. To establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest all of the claim limitations. As discussed above, neither Saldanha nor Serta alone or when combined teaches or suggests all the claim limitations of claim 1. Claims 22-27

depend from claim 1 and are allowable over Saldanha and Serta for at least the same reasons. Gupta does not cure the deficiencies of Saldanha in view of Serta.

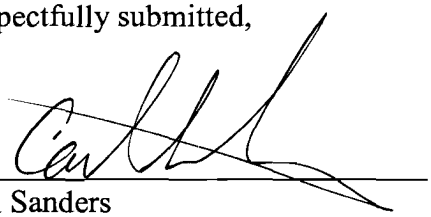
Claims 22-27 depend from claim 1. In claim 1, as amended, Applicant claims "[a] processor comprising: a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations; [and] a plurality of registers, wherein the plurality of registers include an instruction register, a next operation address register, and an end of OR address register." None of Saldanha, Serta, and Gupta alone or when combined teaches or suggests "[a] processor comprising: a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations; [and] a plurality of registers, wherein the plurality of registers include an instruction register, a next operation address register, and an end of OR address register." Thus claim 1 is allowable over Saldanha in view of Serta and further in view of Gupta. Since claims 22-27 depend from claim 1, claims 22-27 are allowable as well. Applicant respectfully requests the Examiner withdraw the rejection of claims 22-27.

VI. Conclusion

Applicants respectfully submit that claims 1-27 are allowable. A favorable Office Action is respectfully solicited.

Should the Examiner have any comments, questions or suggestions of a nature necessary to expedite the prosecution of the application or to place the case in condition for allowance, the Examiner is courteously requested to telephone the undersigned at the number listed below.

Respectfully submitted,



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Carl Sanders
Registration No. 57,203

KILPATRICK STOCKTON LLP
1001 West Fourth Street
Winston-Salem, North Carolina 27101-2400
Telephone: (336) 607-7311
Facsimile: (336) 734-2621